EVOLUTION AND APPLICATIONS OF SYSTEM ON A CHIP SPACEWIRE COMPONENTS FOR SPACEBORNE MISSIONS

Session: SpaceWire Components

Long Paper

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ABSTRACT

As reported at the first SpaceWire International Conference in 2007, BAE Systems in conjunction with NASA has created and space qualified a radiation hardened SpaceWire system on a chip ASIC containing a four port SpaceWire router, embedded microcontroller and memory, built-in memory, discrete, test and dual PCI interfaces. This ASIC has been inserted into a number of missions, including both the single board computer and the Mini-RF payload for the Lunar Reconnaissance Orbiter (LRO) NASA Mission planned for launch in November 2008. This versatile ASIC also supports creating routers scalable beyond its four ports. The SpaceWire core has been updated by NASA and was integrated with other ASIC functions into BAE Systems' latest RAD750^{TM} bridge ASIC, the Golden Gate, shrinking the number of ASICs required for a Processor with SpaceWire by half.

This paper will describe the BAE Systems' SpaceWire ASIC's use within and between the Mini-RF system and the LRO Spacecraft as well as details about the board containing the ASIC and software supporting it mission. This paper will discuss the latest information on creating and programming larger than 4 port SpaceWire routers using this ASIC. The paper will describe the SpaceWire ASIC Evaluation Board that has been created for prototype development using the ASIC in a COTS chassis. Finally the paper will describe the integration of the SpaceWire core and other functional upgrades that were included in the Golden Gate ASIC, our latest bridge ASIC fabricated for standalone or processor bridge use in Spacecraft processing.